Application No.: 09/873,580 Docket No.: T2171.0196/P196

REMARKS/ARGUMENT

Claims 9-21 are now presented for examination. Claims 9 and 18 have been amended. Claims 19-21 have been added to provide Applicant with a more complete scope of protection.

Claims 9 and 20 are the only independent claims.

Japanese document JP-A 2-58261 was cited in the Information Disclosure Statement filed with the initial filing papers of this application. However, the Examiner did not consider the reference on the grounds that a copy had not been provided. As was previously pointed out in the Amendment dated March 12, 2002, no copy of the reference was required since the reference was originally cited in the parent application to which the is application claims benefit under 35 U.S.C. §120. In view of this fact, it is requested that the Examiner initial a new copy of the form PTO-1449 so as to indicate consideration of JP-A 2-58261.

Applicant represents that the cited reference discloses implanting As to the second and third regions (Fig. 1(a)), and implanting B to the third and fourth regions (Fig. 1(b)) to form different threshold voltages. The references shows two step impurity diffusion for the partially overlapped relation. For the convenience of the Examiner, a copy of JP-A 2-58261 is submitted herewith, together with an Abstract obtained online and a fresh copy of the above-mentioned form PTO-1449. It is requested that the initialed form be returned with the next Office Action.

Claims 9-15 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,396,098 (Kim et al.). Claims 16-18 were rejected under 35 U.S.C. § 103 as obvious from Kim et al. in view of U.S. Patent 5,595,922 (Tigelaar et al.). Applicant submits that independent claim 9, and new independent claim 20, are patentable over the cited prior art for

at least the following reasons.

Claim 9 is directed to a method of manufacturing a semiconductor device comprising at least first and second MOS transistors. The method comprises: providing a semiconductor substrate having at least first and second active regions of a first conductivity type; forming a gate oxide layer having a first thickness onto at least the first and second active regions; forming an electrode layer of non-doped polysilicon onto the gate oxide layer; patterning the electrode layer to form first and second gate electrodes onto the first and second active regions, respectively; doping the first active region and the first gate electrode with an impurity of a second conductivity type which is opposite to the first conductivity type to form a first transistor driven at a first voltage level, the first gate electrode being doped at a first concentration; and doping the second active region and the second gate electrode with an impurity of the second conductivity type to form a second transistor driven at a second voltage level lower than the first voltage level, the second gate electrode being doped at a second concentration higher than the first concentration.

Kim et al., as understood by Applicant, forms different source/drain regions for a memory cell transistor and a peripheral transistor. For this purpose, three ion implantation steps are carried out. Kim et al. forms a polycide (polysilicon/silicide) gate electrode or an impurity doped polysilicon gate electrode before the ion implantation steps for forming the source/drain regions (column 4, lines 18-28). The polycide gate electrode has a lower polysilicon layer and an upper silicide layer. The lower polysilicon layer is less influenced by the later ion implantation process. Thus, the lower polysilicon layer should be doped initially. A heavily doped polysilicon gate electrode is also not much influenced by the later ion implantation process because it is or will be saturated with the impurities.

In a later process of Kim et al., the memory cell area is heavily doped with impurity and the peripheral area is less heavily doped with impurity to form many heavily doped source/drain regions for the memory cell and to form heavily doped source/drain regions for

the peripheral transistor. However, the gate electrodes are doped before doping the memory cell area. The impurity concentration of the gate electrode is not greatly changed by the latter doping process, because it is initially doped with high impurity concentration.

In the invention defined by claim 9, the first gate is doped to a first concentration from the non-doped state, while the second gate electrode is doped to a second concentration which is higher than the first concentration, from the non-doped state. This combination of steps positively utilizes this difference of the impurity concentration in the gate electrodes and is not taught by Kim et al.

Claim 11 recites that the lower impurity concentration in the gate electrode enables creation of a depletion layer when the high driving voltage is applied. The Office Action argues that Figs. 9 and 10 of Kim et al. disclose this feature. This is incorrect. Kim et al.'s Figs. 9 and 10 relate to formation of the source/drain regions, not to formation of the gate electrodes.

Claim 10 recites that the doping steps comprise implanting impurities in the active regions and gate electrodes. This step is illustrated in Fig. 4E or 4F. At this stage, the second active region has the same concentration as the first active region. The second active region requires additional implantation step as shown in Fig. 4H or 4I. That is, the low impurity concentration region is first made and the high impurity concentration region is made thereafter.

Claim 20 is directed to a method of manufacturing a semiconductor device. The method comprises: (a) doping a high voltage circuit at a low impurity concentration; and (b) doping a low voltage circuit at a high impurity concentration after the step (a). Claim 21, further comprises: (c) forming a sidewall spacer after the step (a) and before the step (b).

In Kim et al., the whole substrate is doped in Fig. 9, then only the memory cells are

doped in Fig. 10, side wall spacers are made on the side wall of the gate electrode in Fig. 11, and then the whole substrate is doped in Fig. 12. Therefore, the peripheral region is twice doped, and the memory cell region is thrice doped. The memory cell region has a higher impurity concentration. The memory cell region is first formed to be high impurity concentration, then the both regions are doped to adjust the impurity concentration.

In Kim et al., a series of doping steps will form heavily doped regions which penetrate beneath the gate electrode in the memory region. The source/drain regions penetrating below the gate electrode make the effective channel to be shorter. The turn-on voltage becomes low. It is effective to lower the power consumption of the memory cell.

When sidewall spacers are formed between the two implantation steps (1) and (2), as in claim 21, impurities are not greatly diffused under the gate electrode. When side wall spacers are formed after a first doping step, the second doping step will not greatly increase the impurity concentration below the gate electrode. Impurities do not diffuse much below the gate electrode, and hence the turn-on voltage is not greatly reduced. Yet the turn on/off characteristics can be made stable. Further, since the impurity diffusion is less, the characteristics of the transistors in all regions of the substrate can be made uniform.

In view of the above, the independent claims are believed patentable over the cited references. A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration or reconsideration, as the case may be, of the

patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

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Respectfully submitted,

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